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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,447	07/12/2004	David V. Horak	FIS920040187US1	4446
23550	7590	01/30/2007	EXAMINER	
HOFFMAN WARNICK & D'ALESSANDRO, LLC			MASINICK, MICHAEL D	
75 STATE STREET			ART UNIT	PAPER NUMBER
14TH FLOOR			2125	
ALBANY, NY 12207				
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/30/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/710,447	HORAK ET AL.
	Examiner	Art Unit
	Michael D. Masnick	2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 August 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-30 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-30 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 July 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>7/12/04, 8/16/04</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claims 1-30 are pending in the current application. This is the first office action on the merits.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3-6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Specifically, claims 3, 13, and 24 does not provide continuity with the claim elements from which they depend. The phrase conducting the process on a first process reference wafer..." seems to be stating that you do the steps of claim 1 again, though that does not appear to be the intent of the applicant. These claims should be rewritten to extend the claim elements of claim 1, or rewritten in independent form to more clearly state the intentions of the applicant.
4. Claims 4-6, 14-17, and 25-27 inherit this deficiency and are likewise rejected. These claims are not further treated on the merits as the metes and bounds have not been clearly established, but if rewritten in independent form with the concepts clearly set forth would likely be considered allowable subject matter pending a further search.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication 2002/0155629 to Fairbairn et al.
3. Referring to independent claims 1, 11, and 22, Fairbairn shows a method, system, and computer program product for correcting a deviation of a dimension of a feature from a target in a semiconductor process, the method comprising the steps of: first measuring the feature prior to conducting a process relative to the feature to obtain an incoming feature dimension (Paragraph 0012); conducting the process based on a process model; second measuring the feature after conducting the process to obtain an outgoing feature dimension; determining an origin of any deviation of the outgoing feature dimension from a target structure dimension; and adjusting, according to the origin, at least one of the measuring steps and the process conducting step to correct for any deviation (all shown in Paragraph 0029).
4. Referring to claims 2 and 20, Fairbairn shows wherein the method is carried out on at least one of: a wafer-by-wafer (W2W) basis; a lot-by-lot (L2L) basis; a with-in-wafer (WIW) basis; and a with-in-die (WID) basis (Paragraph 0006).
5. Referring to claim 7, Fairbairn shows wherein at least one of the first and second measuring steps includes adjusting a respective feature dimension to address at least one of: a calibration adjustment and a wafer state deviation (paragraph 0029).

6. Referring to claims 8, 18, and 28, Fairbairn shows the step of feeding forward a process model adjustment to the process conducting step for the process model to address any deviation of the first measurement from the target structure dimension based on the first measurement (0029 – “fed forward to the etcher”).

7. Referring to claims 9, 19, and 29, Fairbairn shows wherein the process model includes a process recipe setting needed to achieve the target dimension from the incoming feature dimension (0029 – “etch recipes”).

8. Referring to claims 10, 21, and 30, Fairbairn shows wherein the measuring steps are carried out using a standalone metrology tool (Title of the patent application).

9. Referring to claims 12 and 23, Fairbairn shows a process reference wafer set including a plurality of process reference wafers that have been generated together, the process reference set including a first process reference wafer that has been run through the process conducting means at a first point in time, and a baseline outgoing feature dimension of the feature from the first process reference wafer has been established at the first point in time (0029 – “test wafers”).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael D. Masinick whose telephone number is (571) 272-3746. The examiner can normally be reached on Mon-Fri, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Leo Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Michael D Masinick
Examiner
Art Unit 2125

MDM, Jan 23, 2007